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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/768,092	02/02/2004	Kozo Makiyama	020212A	8674

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EXAMINER	
POMPEY, RON EVERETT	
ART UNIT	PAPER NUMBER
2812	

DATE MAILED: 09/11/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/768,092	MAKIYAMA ET AL.	
	Examiner	Art Unit	
	Ron E. Pompey	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 July 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5,6 and 12-22* is/are pending in the application.

4a) Of the above claim(s) *5,20 and 21* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 5-6, 12-19 and 22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 6, 12-19 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Anda et al. (US 6051454), in view of Nishimoto et al. (US 4224089) and in further view of Furukawa et al. (US 6387783).

Yoshida discloses the limitations of:

Claim 1: A method of manufacturing a semiconductor device, comprising the steps in the following order:

(a) preparing a semiconductor substrate having current input/output regions (33, 34, fig. 5(c));

(b) forming an insulating layer on the semiconductor substrate (40, fig. 5(c));

(c) forming a resist laminate (35 and 36, fig. 6(a)) on the semiconductor substrate;

(d) forming an upper opening through an upper region (36b, fig. 6(c)) of the resist laminate, the upper opening having a laterally broadening middle space;

(e) forming a lower opening (35b, fig. 6(d)) through a lower region of the resist laminate, the lower opening communicating the upper opening, having a limited size along a current direction, and having generally vertical sidewalls;

(f) etching the insulating layer (40a, fig. 7(a)) exposed in the lower opening to from a gate electrode opening exposing the semiconductor substrate;

(h) filling a gate electrode stem in the gate electrode opening and the lower opening and forming a head (7, fig. 8) in the upper opening, the head having an expanded size along the current direction;

Claim 6: A method of manufacturing a semiconductor device, comprising the steps in the following order:

(a) preparing a semiconductor substrate having;

(b) forming a resist laminate on the semiconductor substrate (35 and 36, fig. 6(a));

(c) forming an upper opening (36b, fig. 6(c)) through an upper region of the resist laminate in each of the plurality of element regions, the upper opening having a laterally broadening middle space;

(d) applying an energy beam (35a, fig. 6(c); col. 12, lns. 13-16) to a lower region of the resist laminate;

(e) forming a lower opening (35b, fig. 6(d)) through the lower region of the resist laminate in each of the element regions, the lower opening communicating the upper opening, having a limited size along a first direction, and having generally vertical side walls; and

(g) filling a conductive stem in the lower opening and forming a head in the upper opening, the head having an expanded size along the first direction (38a and 38b, fig. 7(d));

Claim 14: wherein said step (d) includes the sub-step of: (d-1) applying a first electron beam (36a, fig. 6(b)) to an upper region of the resist laminate, registered with said upper opening;

Claim 15: wherein said step (d) further includes the sub-steps of: (d-2) developing (36b, fig. 6(c)) an upper portion of the resist laminate in the region applied with said first electron beam to form an upper window; and (d-3) etching a middle portion of the resist laminate through said upper window to form said laterally broadening space (col. 12, lns. 1-12);

Claim 16; wherein said step (e) includes the sub-steps of: (e-1) applying a second electron beam (35a, fig. 6(c)) to a lower region of the resist laminate, registered with said lower opening, through said upper window and said laterally broadening space; and (e-2) developing an lower portion of the resist laminate in the region applied with said electron beam to form said lower opening(col. 12, lns. 13-16);

Claim 17: wherein said step (c) contains the sub-steps of: (c-1) coating a lower electron beam resist layer (35, fig. 5(d)) on the insulating layer (40, fig. 6(a)); (c-2) baking the lower electron beam resist layer (col. 11, lns. 33-36); and (c-3) coating a soluble resist layer on the lower electron beam resist layer, and coating an upper electron beam resist layer (36, fig. 6(a)) on the soluble resist layer; and

Claim 22: wherein said energy beam in said step (d) is electron beam (col. 11, ln. 1 – col. 12, ln. 62).

3. Anda reads on the claims as applied above, but does not disclose the claimed limitation(s) of:

Claim 1: (g) performing a heat treatment of the resist laminate to move the side walls (3b, fig. 6) of the lower opening so that at least one of opposite ends of the lower region of the resist at the lower opening is retarded from a corresponding end of the insulating layer and that the lower opening of the resist has a forward taper shape upwardly and monotonically increasing a size of the lower opening along the current direction;

Claim 2: wherein the heat treatment in said step (g) is performed at a temperature lower than a glass transition temperature of the lower region of the resist laminate;

Claim 3: wherein the heat treatment in said step (g) makes the opposite side walls of the lower opening facing in the current direction have a generally symmetric taper shape and be retarded from opposite ends of the insulating layer (col. 3, ln. 39 – col. 4, ln. 22);

Claims 6 and 12: (a) a plurality of element regions;

(d) applying an energy beam to a lower region of said resist laminate in at least part of said plurality of element regions at a different dose depending on the element region;

(f) performing a heat treatment of the resist laminate to deform the side walls of the lower opening in at least some of the element regions in accordance with doses so that the lower opening has a taper shape upwardly and monotonically increasing a size of the lower opening along the first direction;

Claim 13: wherein said step (g) forms the sidewalls of the lower opening having different taper angles.

Claim 18: wherein the heat treatment in said step (g) is performed at a temperature below a glass transition temperature of the lower electron beam resist layer; and

Claim 19: wherein said forward taper shape has a general symmetric taper angle.

However,

a. Nishimoto discloses the above claimed limitations regarding:

Claim 1: (g) performing a heat treatment of the resist laminate to move the side walls (17A, fig. 7) of the lower opening so that at least one of opposite ends of the lower region of the resist at the lower opening is retarded from a corresponding end of the insulating layer and that the lower opening of the resist has a forward taper shape upwardly and monotonically increasing a size of the lower opening along the current direction;

Claim 3: wherein the heat treatment in said step (g) makes the opposite sidewalls of the lower opening facing in the current direction have a generally symmetric taper shape and be retarded from opposite ends of the insulating layer; and

Claim 19: wherein said forward taper shape has a general symmetric taper angle (column(s) 3, line(s) 41-47).

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Anda with Nishimoto, because this will cure the sheet and improve precision during etching.

b. Furukawa discloses the above claimed limitations regarding:

Claim 18: performing a heat treatment on the lower resist at a temperature lower than a glass transition temperature in column 3, ln. 65 – col. 4, ln. 4.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine Anda with Furukawa, because the heat treatment will cure the sheet and improve precision during etching.

a. It would have been obvious to one of ordinary skill in the art at the time the invention was made to make more than one element since it has been held that mere duplication of essential working parts of a device involves only routine skill in the art. *St. Regis Paper Co. v. Bemis Co.*, 193 USPQ 8.

Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention that more than one element could be formed simultaneously to allow faster production of devices.

Also, It would have been obvious to one of ordinary skill in the art at the time the invention was made to use different doses on the lower resist region, because the different doses provide for precise tailoring of opening dimensions, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only ordinary skill in the art. *In re Aller*, 105 USPQ 233.

Election/Restrictions

4. Newly submitted claims 5 and 20-21 are directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: Claims 5 and it dependent claims 20-21, pertain to an invention that was not elected in the response received on July 14, 2005.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claims 5 and 20-21 are withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

Response to Arguments

2. Applicant's arguments with respect to claims 1-3, 6, 12-19 and 22 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E. Pompey whose telephone number is (571) 272-1680. The examiner can normally be reached on 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Ron Pompey
AU: 2812
September 3, 2006

MICHAEL LEBENTRITT
SUPERVISORY PATENT EXAMINER